REMARKS

Per the objection to claims 14 and 15, it is noted that claim 14 refers to operating and resampling being performed while a mobile station is tuned to a desired RF frequency channel, while claim 15 states that operating and resampling are performed while the mobile station is tuned to a desired RF frequency band. A frequency band can comprise multiple frequency channels (see also page 8, lines 4-9, of the specification). As such, claims 14 and 15 are not duplicate claims.

Claims 5, 9 and 10 were rejected under 35 U.S.C. 112, second paragraph for the reasons of record. While not admitting that the language noted by the Examiner is ambiguous or unclear, the language has been removed from claims 5 and 9, and claim 10 has been cancelled without prejudice. The Examiners rejection is thus rendered moot by this amendment.

Claims 1, 2, 3, 5, 6, 7, 9, 11 and 12 were rejected under 35 U.S.C. 102(b) as being anticipated by Cok et al. (U.S. 4,573,023), while claims 4, 8 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cok et al. in view of Hunt, Jr. et al. (U.S. 6,385,276). Claims 14-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cok et al., as applied to claim 9. These rejections are respectfully disagreed with, and are traversed below. It will be shown below that the resemblances between the circuitry shown in the prior art that was relied upon by the Examiner, and this invention, is primarily superficial.

In order to advance this patent application to issuance, claims 1 and 10 have been cancelled without prejudice, and claims 2, 4, 5, 8, 9 have been amended. Claim 2 now recites, in part, that the at least one resampling stage is:

> "comprised of a flip-flop having a data input coupled to said output of said at least one of said divider stages and a clock input coupled to said input node for being clocked with said output of said voltage controlled oscillator".

Independent claims 5 and 9 have been amended along similar lines.

The prior art that has been cited and relied upon by the Examiner is not seen to expressly disclose or suggest this subject matter. Cok et al. do show D-type flip-flops in Fig. 2. However, the first F/F 54 is clocked by the output of the prescaler 50, the D input is driven by the Q- not output, and the Q output clocks the second F/F 62, which receives its D input from the control logic 44. While the Examiner has apparently recognized these deficiencies in the teachings of Cok et al., and cited Hunt, Jr. et al. when rejecting claims 4, 8 and 13, it is noted that the teachings of Hunt, Jr. et al. do not cure the deficiencies in the teachings of Cok et al. For example, the embodiments of Figs. 1 and 5 merely divide an input clock frequency (f_{in}) using a plurality of D-type flip-flops. The first set of flip-flops 545, 550, 557 are all clocked by the input clock frequency, while for the second set of flip-flops 580-1, 580-2, 580-3: flip-flop 580-1 is clocked by the output of flip-flop 550, flip-flop 580-2 is clocked by the output of 580-1, and flip-flop 580-3 is clocked by the output of 580-2. It should be noted that the only external input to the D inputs of these flip-flops is a modulus control signal 570, via decode logic 515 and gate 55 to the D input of flip-flop 557.

It is respectfully pointed out that no combination of Cok et al. and Hunt Jr., et al. meets or suggests the subject matter of the independent claims 2, 5 and 9, as currently presented for examination. This being the case, the Examiner is respectfully requested to reconsider and remove the rejections of claims 2, 5 and 9, as well as all claims that depend from claims 2, 5 and 9, and to allow these claims as they are presently submitted for examination.

Claims 17-21 are newly added, and are also patentable over the prior art that was cited and relied upon by the Examiner.

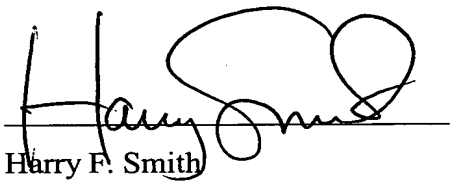
For example, claim 17 is drawn to a mobile station and includes:

> "a prescaler block disposed between an output of said VCO and an input of a frequency divider, said prescaler block comprising a frequency divider block having an input coupled to said output of said VCO, said frequency divider block having an output for outputting a frequency divided signal, said prescaler block further comprising a flip-flop having an input coupled to said output of said frequency divider block and a clock input coupled to said output of said VCO,

said flip-flop operating to cause said prescaler block to output to said frequency divider a prescaled VCO signal having edge transitions that are synchronized to edge transitions of the VCO output signal." (emphasis added)

The prior art that was cited and relied upon by the Examiner is not seen to expressly disclose or suggest at least the subject matter that is highlighted above. A favorable consideration that results in the allowance of claims 17-21 is also earnestly solicited.

Respectfully submitted:



3/26/2003

Harry F. Smith — Date

Reg. No.: 32,493

Customer No.: 29683

HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212

Telephone: (203)925-9400
Facsimile: (203)944-0245
email: hsmith@hspatent.com